

HP3580A 100kHz synchronously tuned filter data
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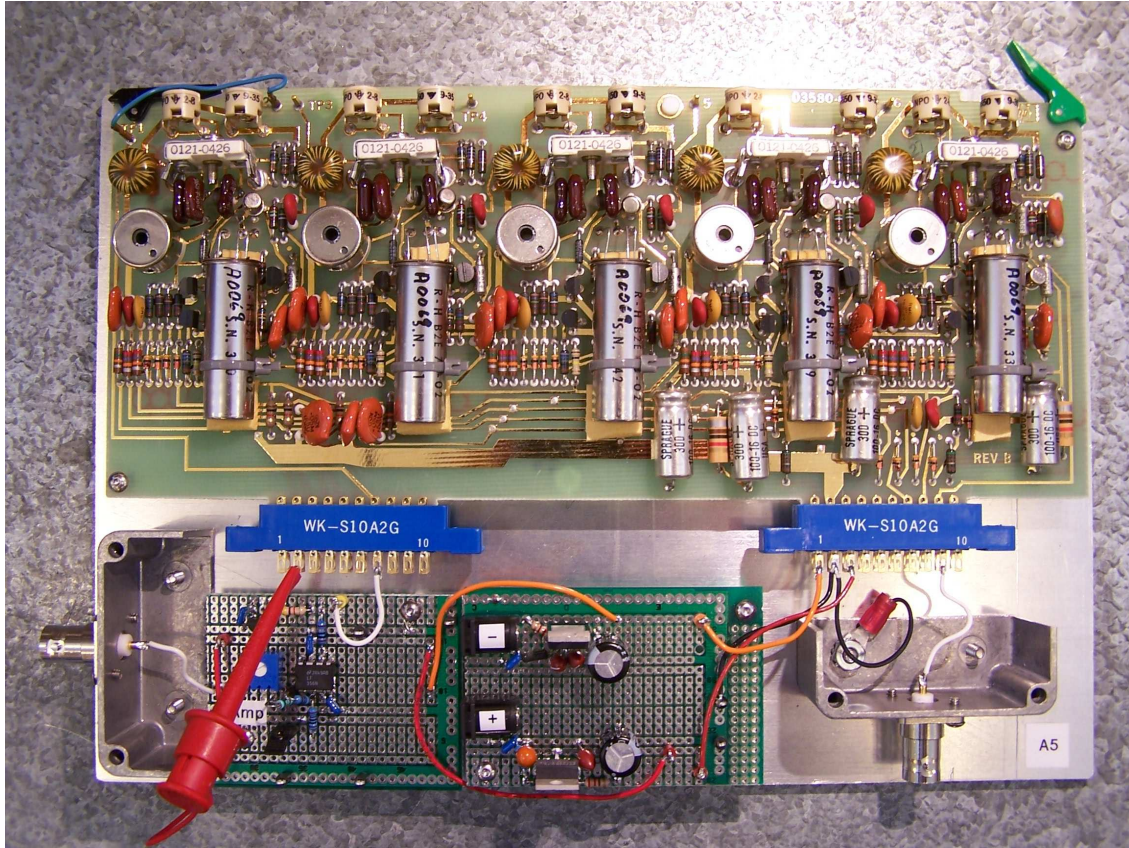


Figure 1: Test fixture for the A5 board from the HP 3580A SA.

With all CTL lines floating, filter is in 300Hz setting. 10VDC gets tied to each individual control line to activate that particular filter bandwidth setting.

+10VDC supply, A5 board draws 4.6mA.

-10VDC supply, A5 board draws < 10mA (not well current monitored)

Table 1 gives the summary of the bandpass filter performance in each bandwidth mode.

Parameter	300 Hz	100 Hz	30 Hz	10 Hz	3 Hz	1 Hz
Center Frequency, Hz	100,104.0	100,010.0	100,001.0	100,000.4	100,000.2	100,000.0
Output at Center Frequency, dBm	1.6	-0.2	-7.3	-9.4	-16.8	-17.9
BW 3dB, Hz	264	98	30	10	3.2	1.2
BW 6dB, Hz	380	142	43	14.6	4.7	1.6
BW 60dB, Hz	2,380	964	295	99.8	31.5	11.1
SF (60dB, 6dB)	6.26	6.79	6.86	6.84	6.71	6.94

Table 1: Summary table of measured crystal filter performance.

Following figures and text show the bandpass performance of the IF filter in each of the 6 selected bandwidths.

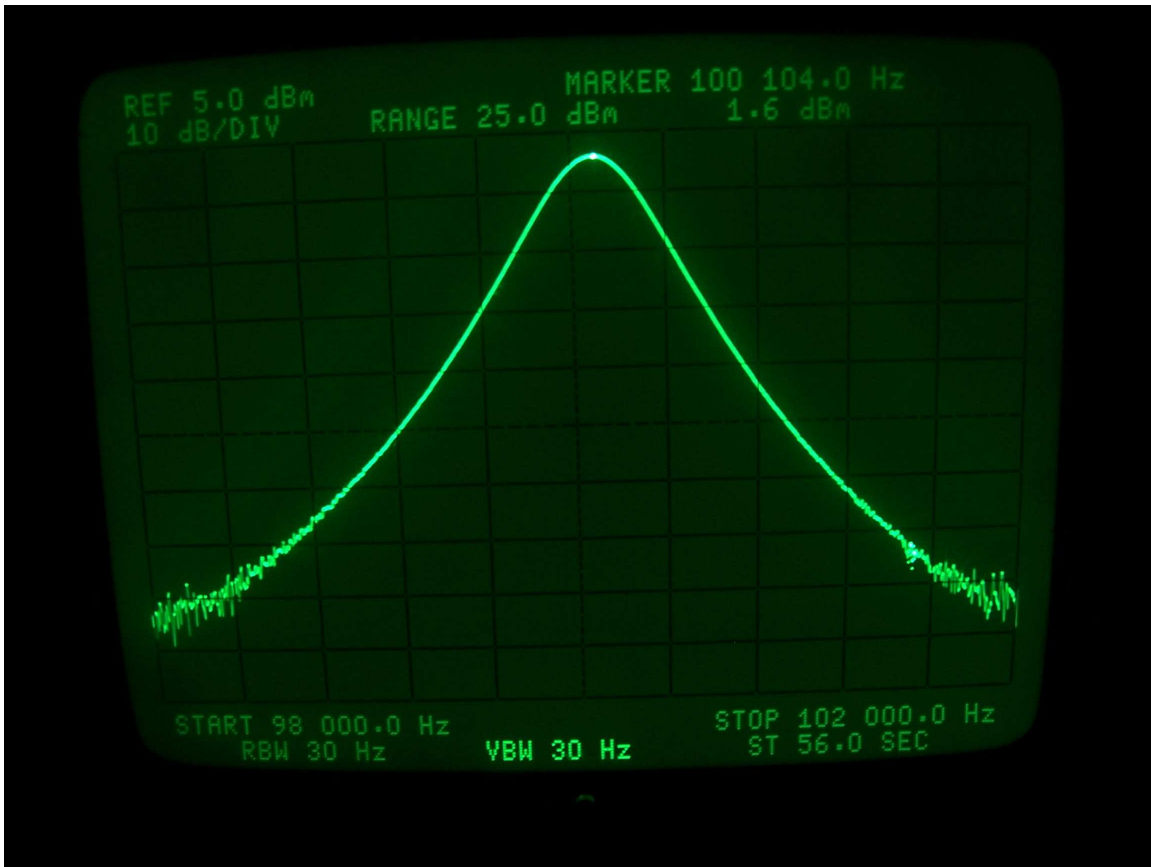


Figure 2: 300Hz setting.

$V_{in} = 640\text{mV}_{pp}$, Step = 400 Hz/div

Center: 100,104.0 Hz, 1.6 dBm

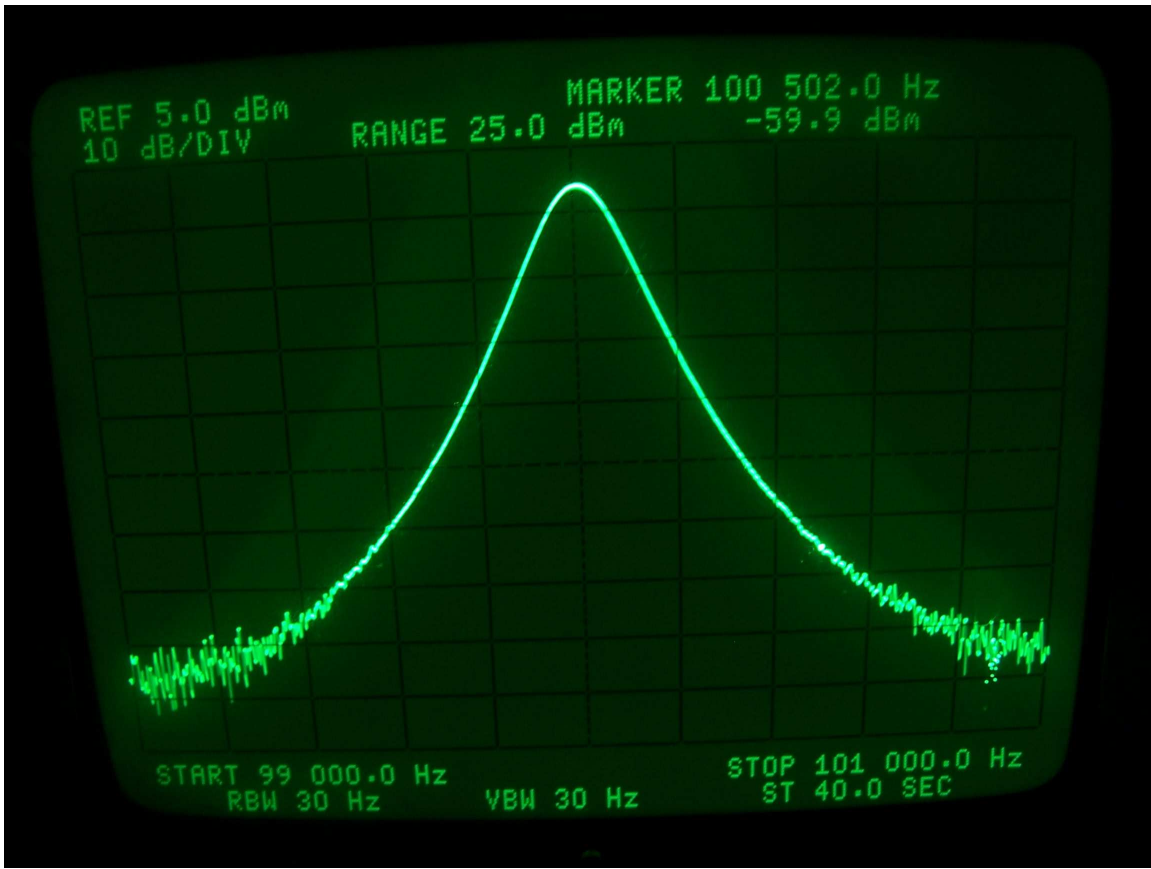


Figure 3: 100Hz setting.

Vin = 640mVpp, Step = 200 Hz/div

Center: 100,010.0 Hz, -0.2 dBm

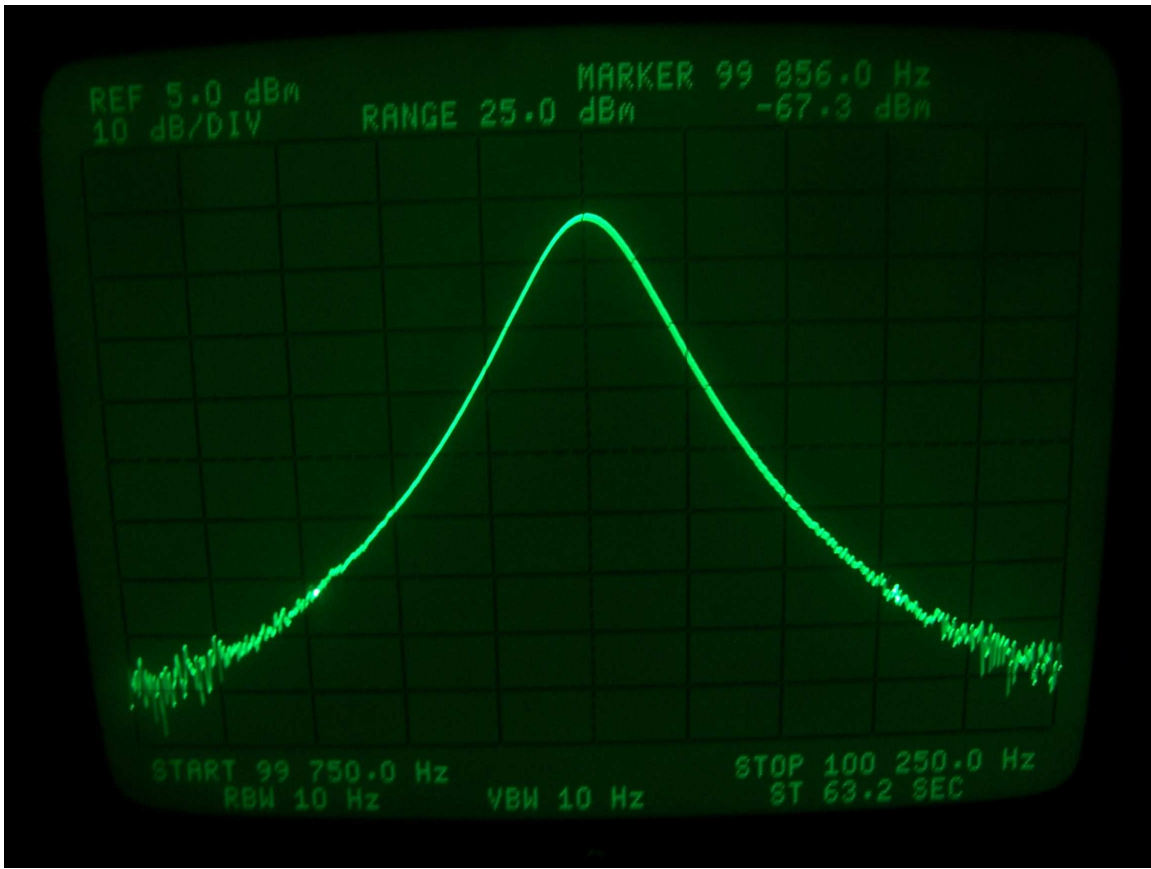


Figure 4: 30Hz setting.

$V_{in} = 332\text{mV}_{pp}$, Step = 50 Hz/div

Center: 100,001.0 Hz, -7.3 dBm

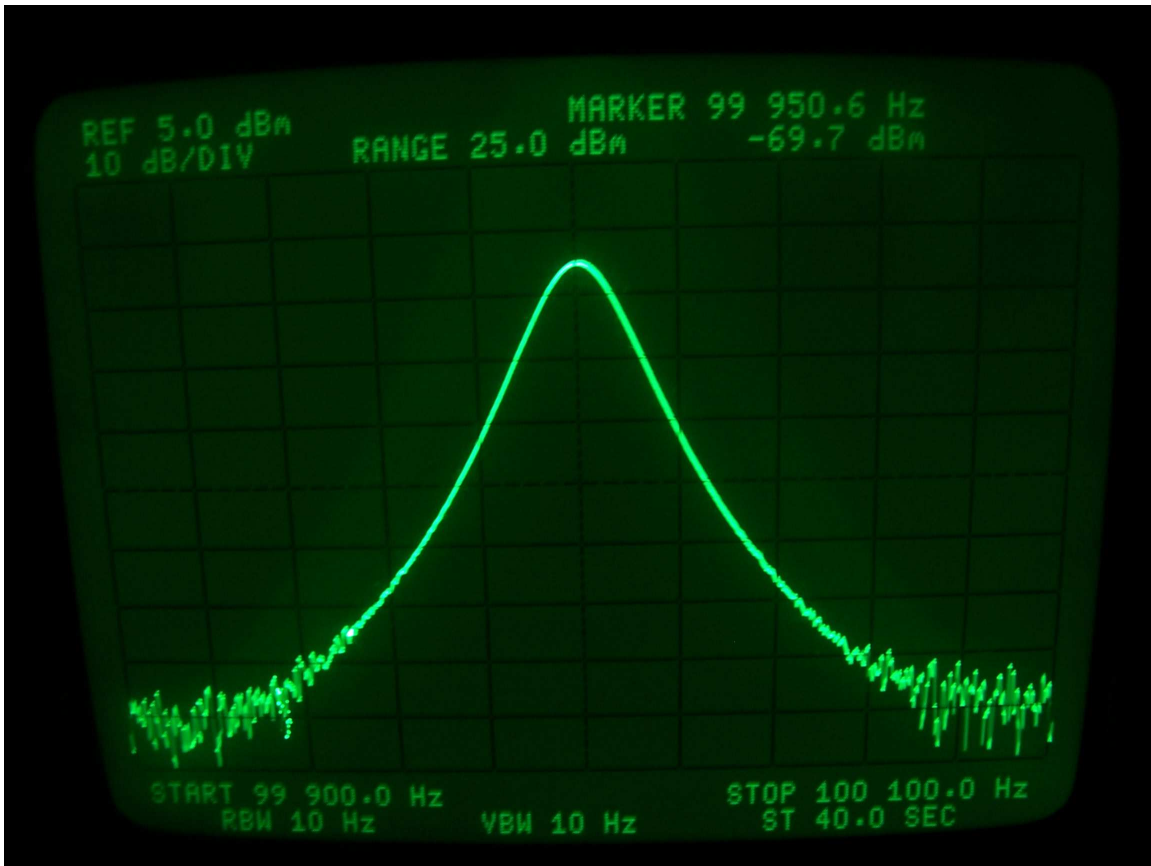


Figure 5: 10Hz setting.

$V_{in} = 332\text{mV}_{pp}$, Step = 20 Hz/div

Center: 100,000.4 Hz, -9.4 dBm

3 Hz and 1 Hz settings not tested yet because V_{in} needs to be reduced below what my buffer design could produce (110mV_{pp}). This will be fixed and I will get data on the last two settings.

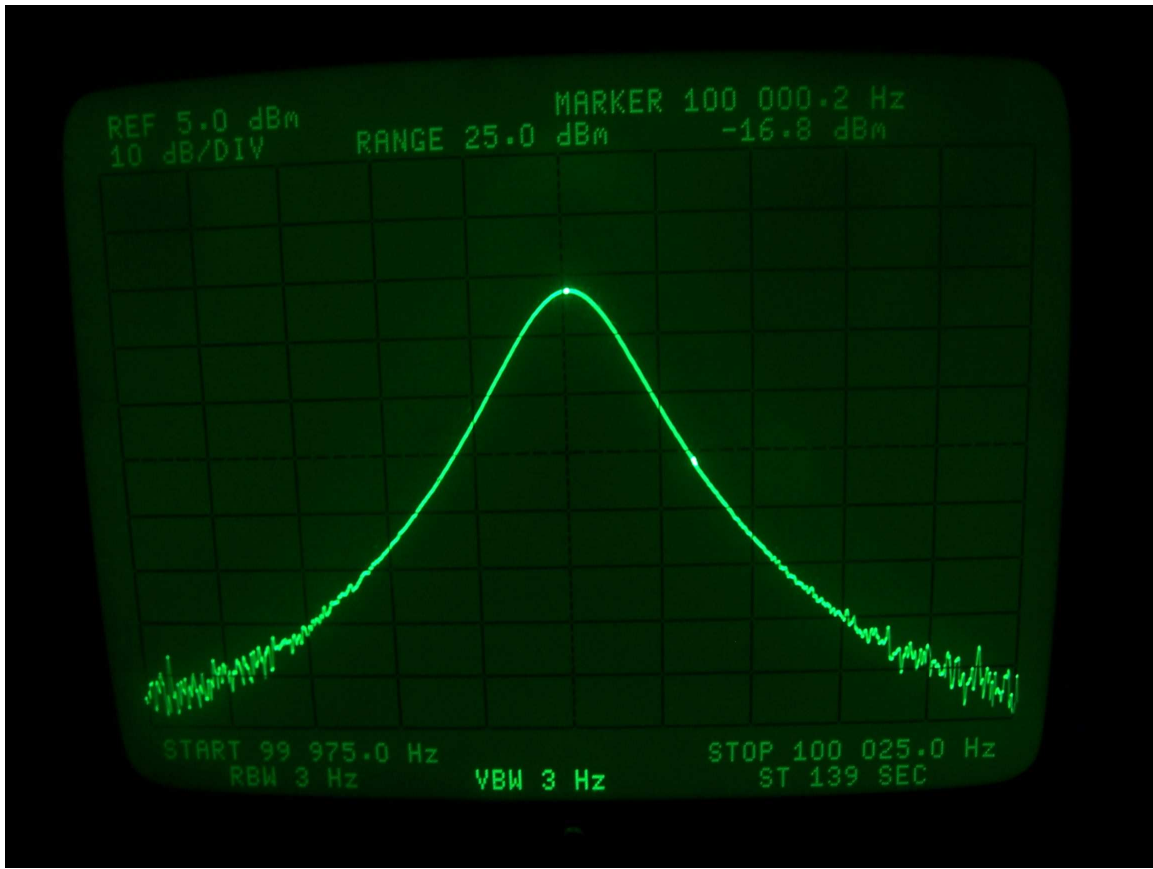


Figure 6: 3Hz filter setting.

Vin = 110mVpp, Step = 5 Hz/div

Center: 100,000.2 Hz, -16.8 dBm

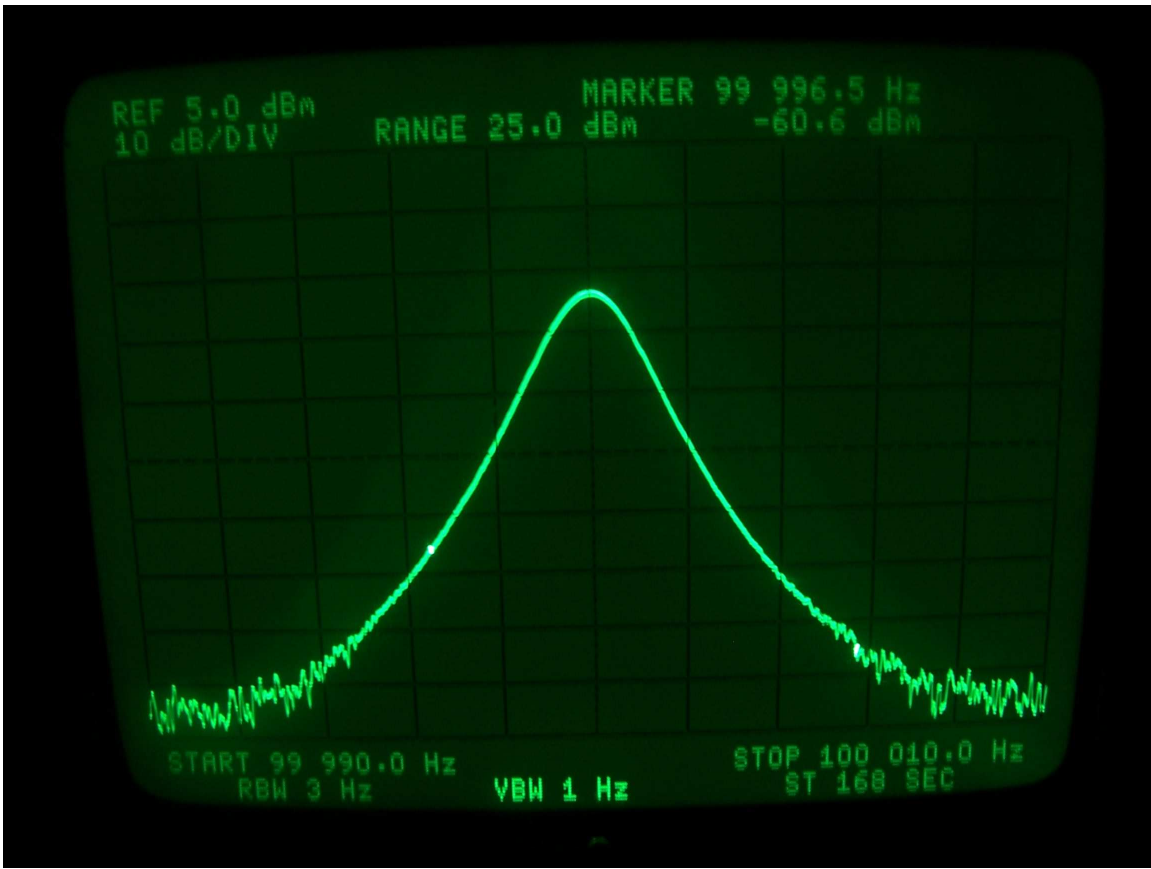


Figure 7: 1Hz filter setting.

$V_{in} = 110\text{mV}_{pp}$, Step = 2 Hz/div

Center: 100,000.0 Hz, -17.9 dBm